



General Description

It combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$.

Features

- Low $R_{DS(ON)}$ to minimize conductive loss
- Low Gate Charge for fast switching
- Low Thermal resistance

Application

- BLDC Motor driver
- DC-DC
- Load Switch

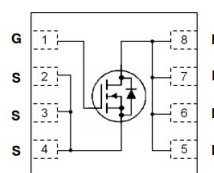
Ordering Information:

Part NO.	ZMS004N04HG
Marking	ZMS004N04H
Packing Information	REEL TAPE
Basic ordering unit (pcs)	2500

Absolute Maximum Ratings ($T_C=25^\circ\text{C}$)

Parameter	Symbol	Conditions	Value	Unit
Drain-Source Voltage	V_{DS}		40	V
Gate-Source Voltage	V_{GS}		± 20	V
Continuous Drain Current	I_D	$T_C=25^\circ\text{C}$	475	A
	I_D	$T_C=75^\circ\text{C}$	388	A
	I_D	$T_C=100^\circ\text{C}$	336	A
Pulsed Drain Current	I_{DM}	Pulsed; $t_p \leq 10 \mu\text{s}$; $T_{mb} = 25^\circ\text{C}$;	1425	A
Total Power Dissipation	P_D	$T_C=25^\circ\text{C}$	250	W
Total Power Dissipation	P_D	$T_A=25^\circ\text{C}$	4.3	W
Operating Junction Temperature	T_J		-55 to +175	$^\circ\text{C}$
Storage Temperature	T_{STG}		-55 to +175	$^\circ\text{C}$
Single Pulse Avalanche Energy	E_{AS}	$L=0.1\text{mH}$, $V_{GS}=10\text{V}$, $R_g=25\Omega$,	560	mJ
		$L=0.5\text{mH}$, $V_{GS}=10\text{V}$, $R_g=25\Omega$,	1176	mJ
ESD Level (HBM)	CLASS 2			

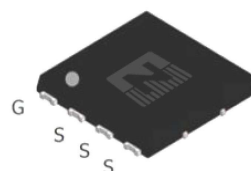
Product Summary



$$V_{DS} = 40\text{V}$$

$$R_{DS(ON)} = 0.45\text{m}\Omega$$

$$I_D = 475\text{A}$$



DFN8*8





•Thermal resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case	R_{thJC}		-	0.6	°C/W
Thermal resistance, junction-ambient	R_{thJA} ①		-	35	°C/W
Soldering temperature	T_{sold}		-	260	°C

•Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	40			V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	2.0	2.7	4.0	V
Drain-Source Leakage Current	I_{DSS}	$V_{GS}=0V, V_{DS}=40V$			1.0	μA
Gate- Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$			100	nA
Static Drain-source On Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=40A$		0.45	0.65	m Ω
Forward Transconductance	g_{FS}	$V_{GS}=5V, I_{SD}=20A$		60		S
Diode Forward Voltage	V_{FSD}	$V_{GS}=0V, I_{SD}=40A$			1.3	V

•Dynamic characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	C_{iss}	$f=1MHz, V_{DS}=25V$	-	10860	-	pF
Output capacitance	C_{oss}		-	3040	-	
Reverse transfer capacitance	C_{rss}		-	168	-	
Gate Resistance	R_g	$f=1MHz$	-	3.2		Ω
Total gate charge	Q_g	$V_{DD}=15V,$ $I_D=40A,$ $V_{GS}=10V$	-	174	-	nC
Gate - Source charge	Q_{gs}		-	42	-	
Gate - Drain charge	Q_{gd}		-	38	-	
Turn-ON Delay time	$t_{D(on)}$	$V_{GS}=10V, V_{DS}=15V,$ $R_G=3.3\Omega, I_D=20A$	-	75	-	ns
Turn-ON Rise time	t_r		-	78	-	ns
Turn-Off Delay time	$t_{D(off)}$		-	120	-	ns
Turn-Off Fall time	t_f		-	55	-	ns
Reverse Recovery Time	t_{RR}	$V_{DD}=20V, dI_S/dt =$ $100A/\mu s, I_S=50A$	-	96	-	ns
Reverse Recovery Charge	Q_{RR}		-	230	-	nC



Fig.1 Gate-Charge Characteristics

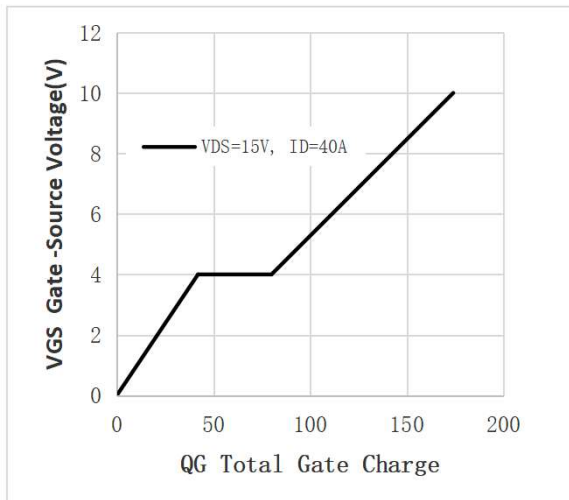


Fig.2 Capacitance Characteristics

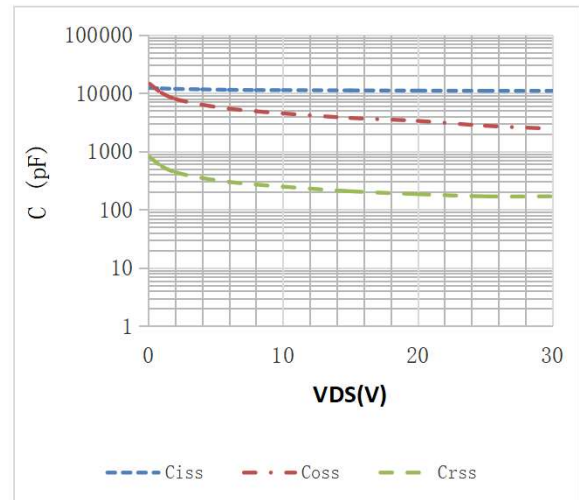


Fig.3 Power Dissipation

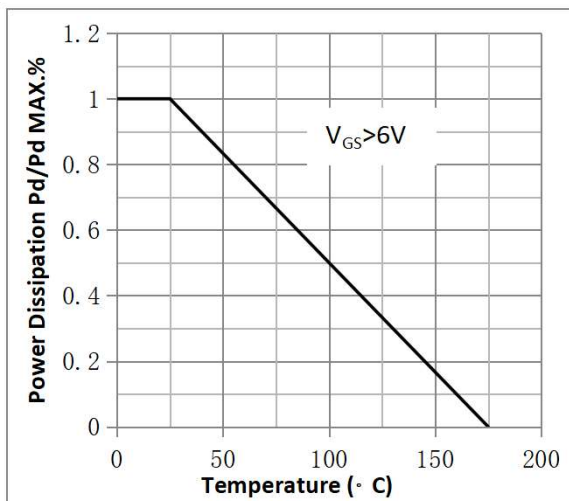


Fig.4 Typical output Characteristics

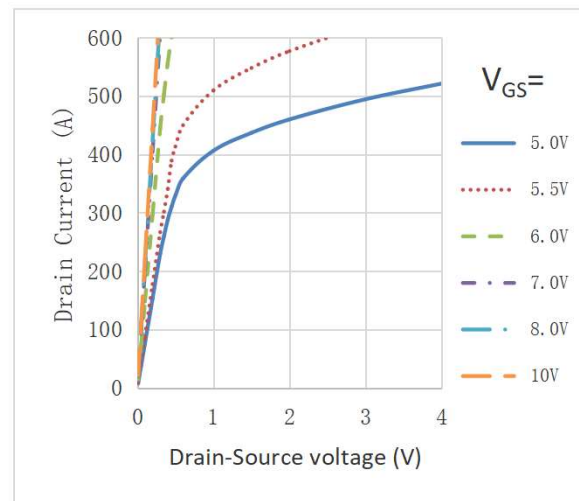


Fig.5 Threshold Voltage V.S Junction Temperature

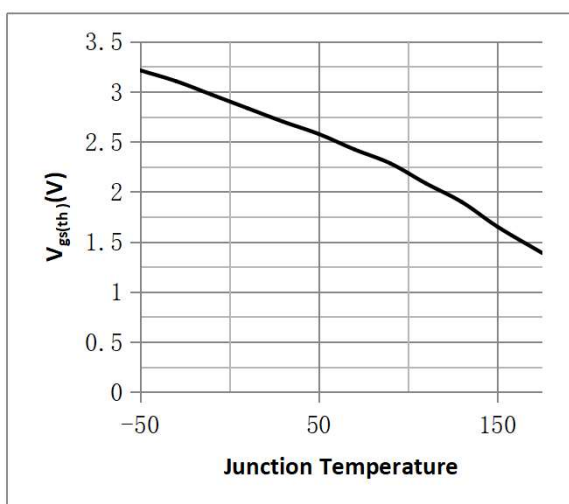


Fig.6 Resistance V.S Drain Current

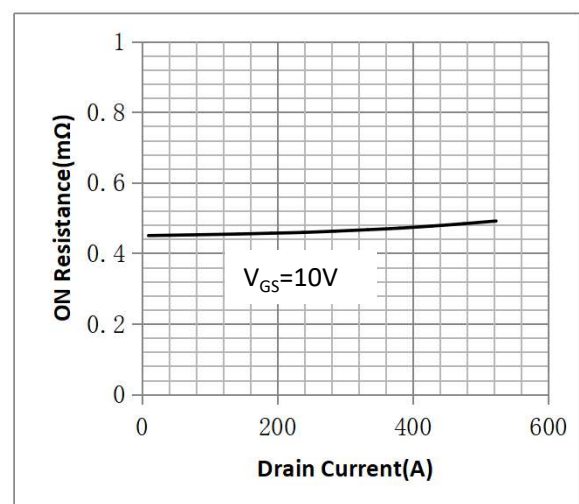




Fig.7 On-Resistance VS Gate Source Voltage

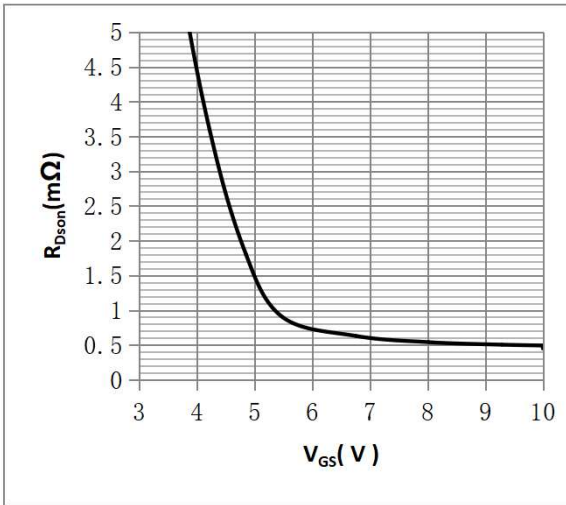


Fig.8 On-Resistance V.S Junction Temperature

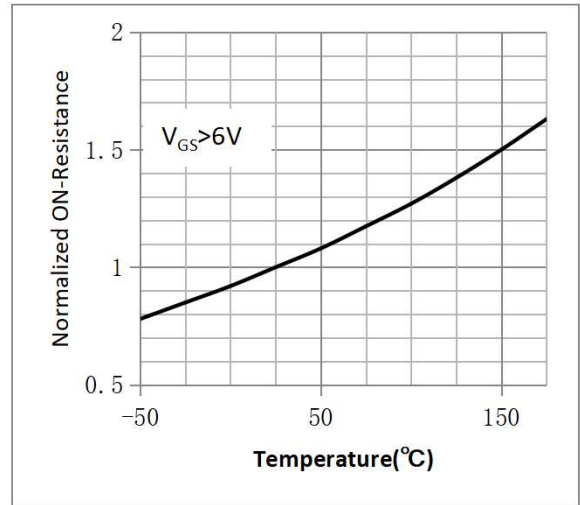


Figure 9. Diode Forward Voltage vs. Current

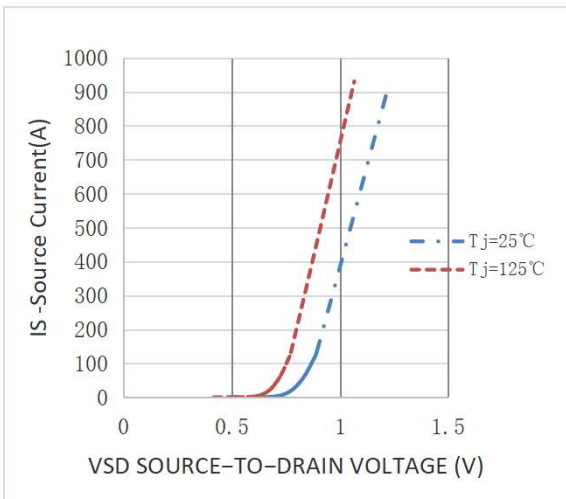


Figure 10. Transfer Characteristics

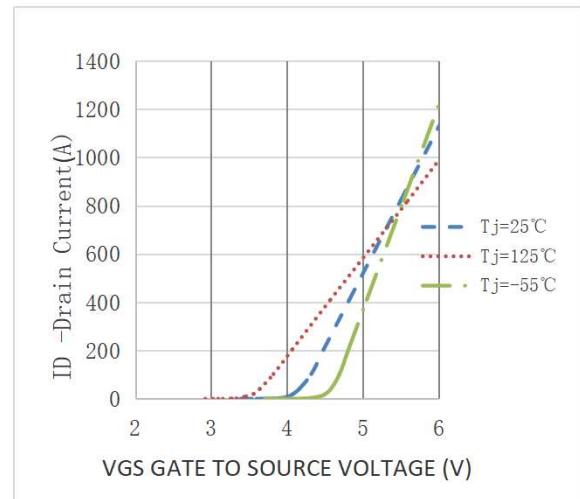
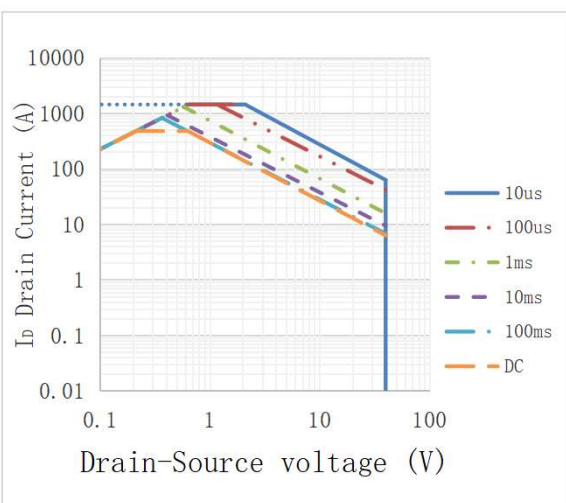
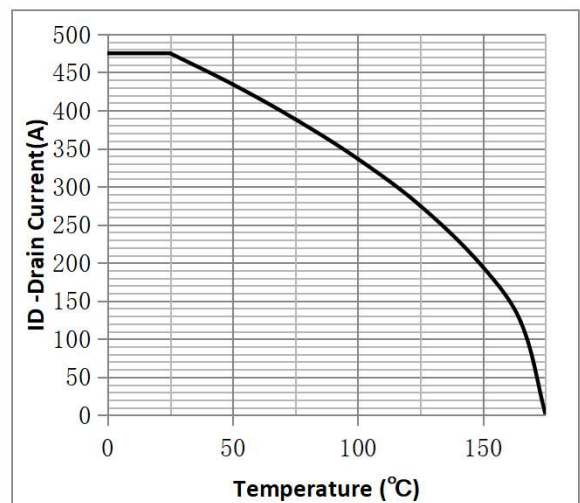
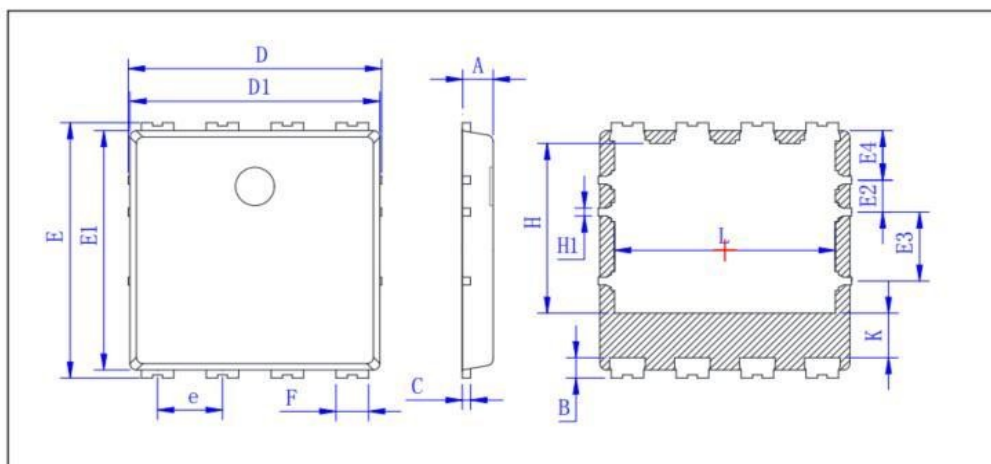


Fig.11 Safe Operating Area

Fig.12 ID vs. Case Temperature^②



•DFN8*8 Package Outline



Symbol	Min	Typ	Max
A	0.90	0.95	1.00
B	0.50	0.60	0.70
C	0.254 TYP		
D	7.70	7.80	7.90
D1	7.60	7.70	7.80
E	7.90	8.00	8.10
E1	7.40	7.50	7.60
E2	0.90	1.00	1.10
E3	2.06	2.16	2.26
E4	1.45	1.55	1.65
e	2.0 TYP		
F	1.00 TYP		
H	5.15	5.30	5.40
H1	0.20	0.25	0.35
L	6.60	6.80	6.90
K	1.20		



Note:

- ① Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate;
- ② Practically the current will be limited by PCB, thermal design and operating temperature. VGS=10V.

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Revision History

Version	Date	Change
A	2022.11.6	new
B	2022.12.8	1.ID and ID curve Modified
C	2023.12.18	Corect SOA Curve



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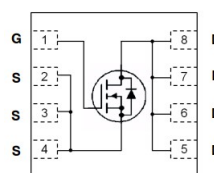
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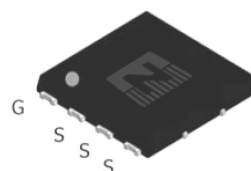
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DFN8*8





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Reverse transfer capacitance	C_{rss}		-	168	-	
Gate Resistance	R_g	$f=1MHz$	-	3.2		Ω
Total gate charge	Q_g	$V_{DD}=15V,$ $I_D=40A,$ $V_{GS}=10V$	-	174	-	nC
Gate - Source charge	Q_{gs}		-	42	-	
Gate - Drain charge	Q_{gd}		-	38	-	
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Turn-ON Rise time	t_r		-	78	-	ns
Turn-Off Delay time	$t_{D(off)}$		-	120	-	ns
Turn-Off Fall time	t_f		-	55	-	ns
Reverse Recovery Time	t_{RR}	$V_{DD}=20V, dI_S/dt =$ $100A/\mu s, I_S=50A$	-	96	-	ns
Reverse Recovery Charge	Q_{RR}		-	230	-	nC



Fig.1 Gate-Charge Characteristics

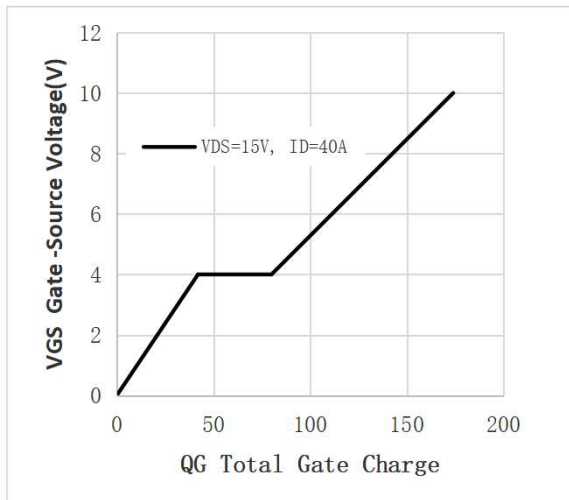


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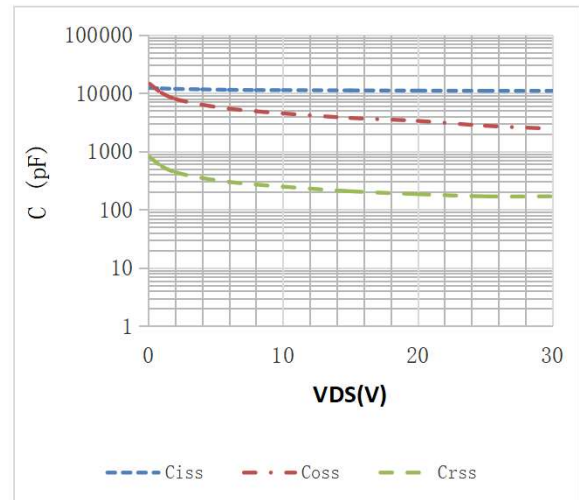


Fig.3 Power Dissipation

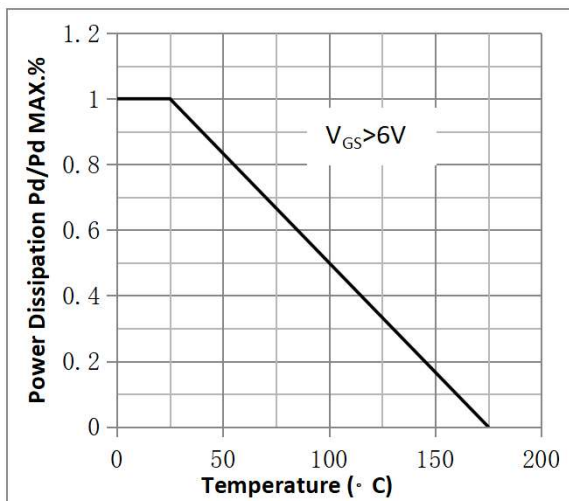


Fig.4 Typical output Characteristics

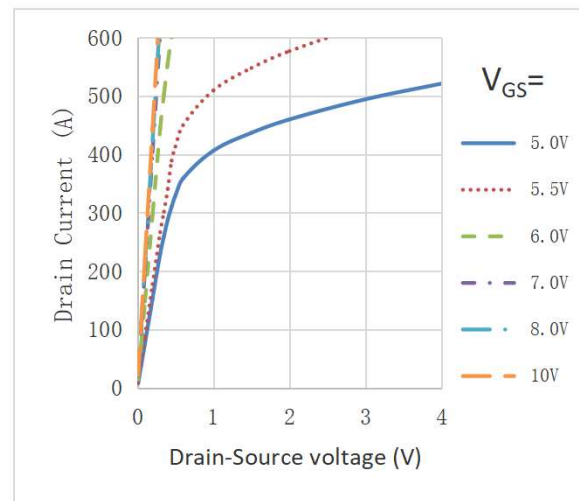


Fig.5 Threshold Voltage V.S Junction Temperature

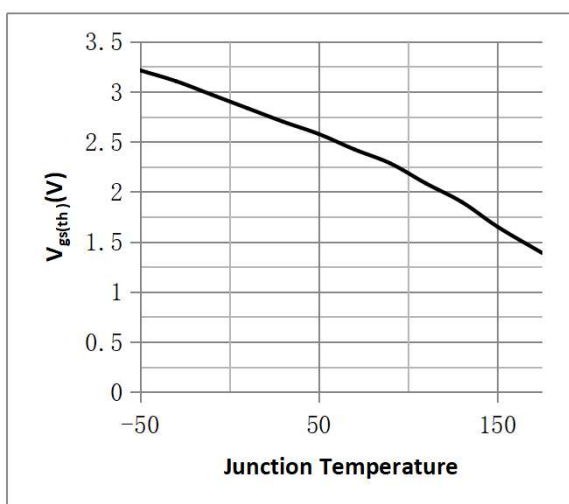


Fig.6 Resistance V.S Drain Current

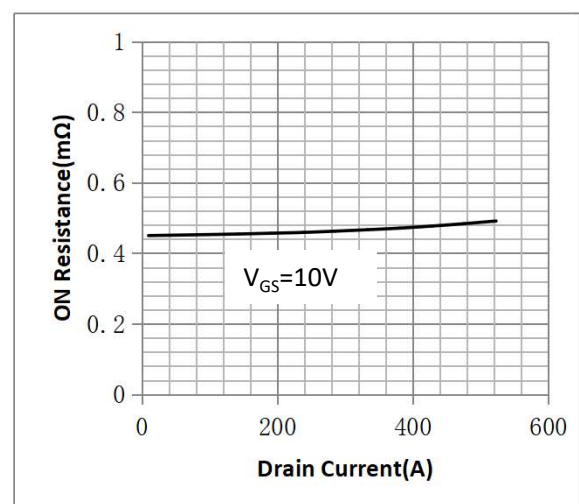




Fig.7 On-Resistance VS Gate Source Voltage

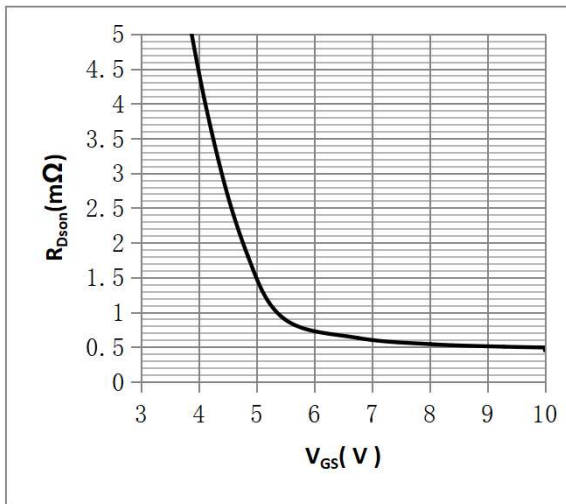


Fig.8 On-Resistance V.S Junction Temperature

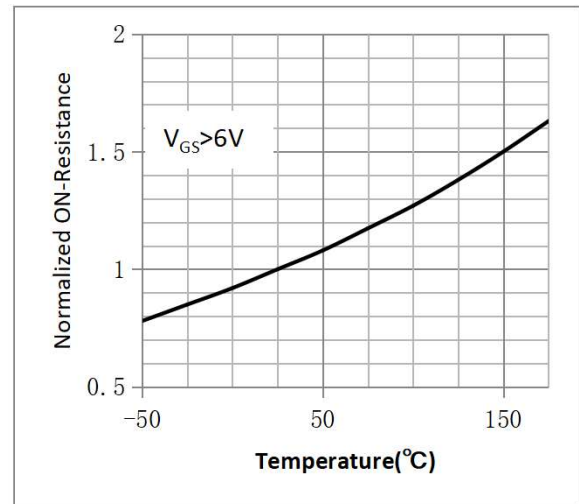


Figure 9. Diode Forward Voltage vs. Current

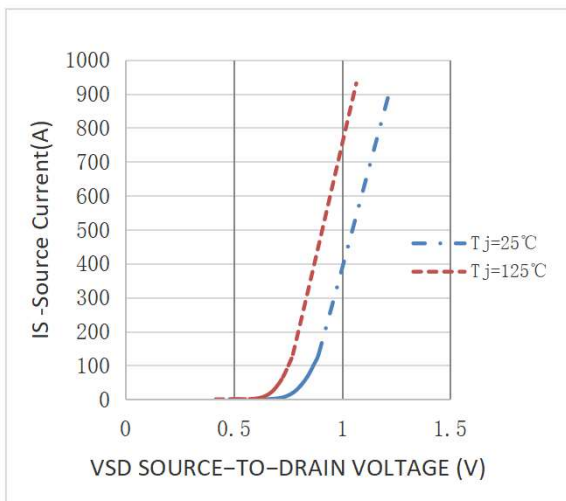


Figure 10. Transfer Characteristics

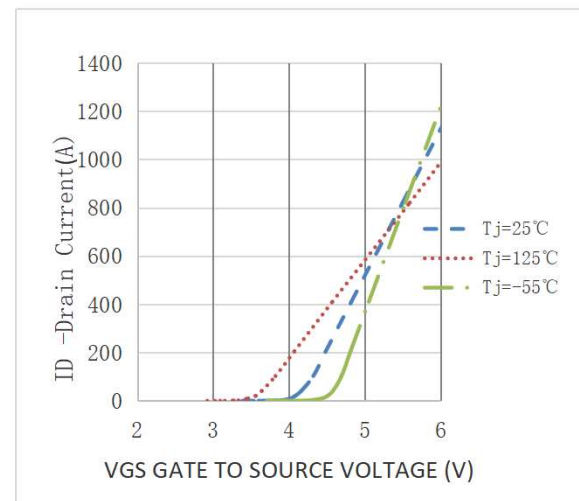
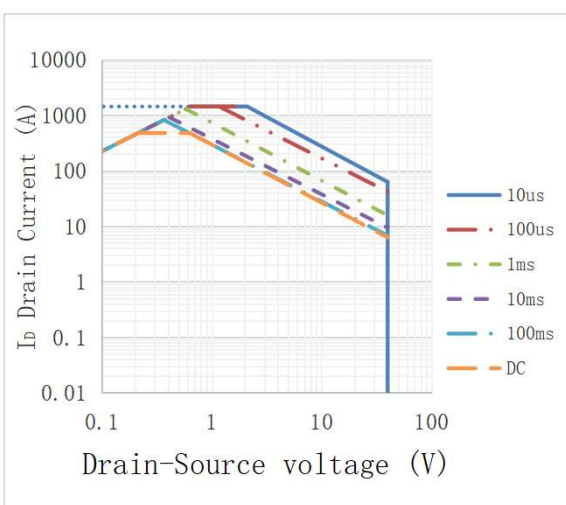
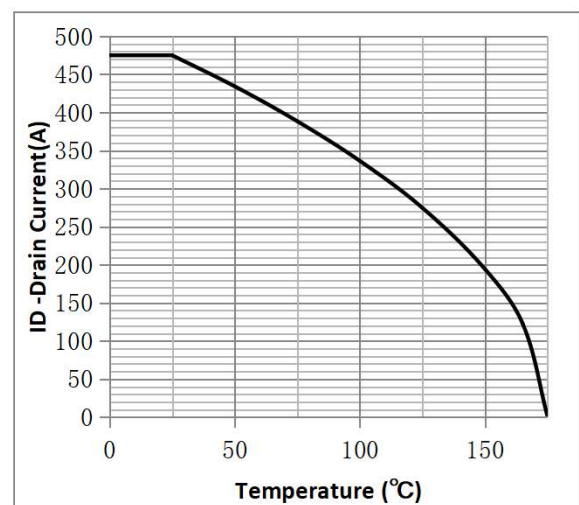
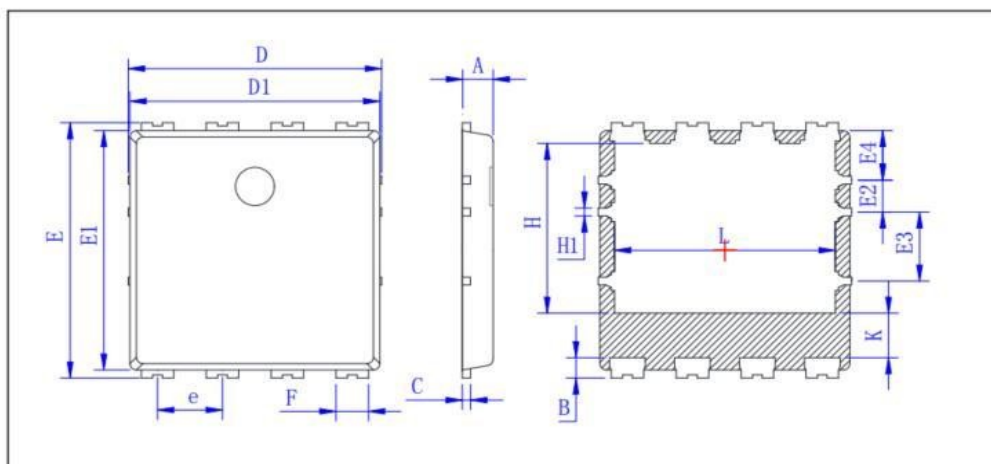


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Fig.12 ID vs. Case Temperature^②



•DFN8*8 Package Outline



Symbol	Min	Typ	Max
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E	7.90	8.00	8.10
E1	7.40	7.50	7.60
E2	0.90	1.00	1.10
E3	2.06	2.16	2.26
E4	1.45	1.55	1.65
e	2.0 TYP		
F	1.00 TYP		
H	5.15	5.30	5.40
H1	0.20	0.25	0.35
L	6.60	6.80	6.90
K	1.20		



Note:

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- ② Practically the current will be limited by PCB, thermal design and operating temperature. VGS=10V.

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